

WHAT IS CLAIMED IS:

1 1. An digital circuit having at least first and second edge-triggered
2 devices, respectively receiving first and second clock signals, and a selectable circuit path
3 for forming at least one scan path that includes the first and second edge-triggered
4 devices, including:

5 a latch in the scan data path, the latch having a data input coupled to
6 receive an output from the first device and an output coupled to an input of the second
7 device, the latch being clocked by the second clock signal to temporarily hold data while
8 the first and second devices change state.

1 2. The digital circuit of claim 1, including multiplexer circuits for
2 selectively forming the scan data path in response to a test signal.

1 3. The digital circuit of claim 2, wherein the first and second devices
2 form functional circuits in absence of the test signal.

1 4. The digital circuit of claim 1, wherein the first and second clock
2 signals are asynchronous to one another.

1 5. A digital circuit structured to be subjected to scan testing,
2 comprising,
3 a scan data input;
4 a scan data output;
5 at least first and second clock domains each including one or more edge-
6 triggered devices, each clock domain receiving first and second clock signals;
7 a data path selectable in response to a test signal for form a scan data path
8 between the scan data input and the scan data output that includes the first and second
9 with a scan data path portion from an output of the first device to an input of the second
10 device; and
11 a latch in the scan data path portion that is clocked by the second clock
12 signal.

1 6. A method of scan-testing digital logic comprising at least first and
2 second digital circuits having a data path from one to the other and respectively clocked

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- 3 by first and second clock signals, each digital circuit including at least one edge-triggered device, the method including the steps of:
 - 5 providing a latch element in the data path clocked by a test clock;
 - 6 asserting a test signal to cause at least one serial scan chain to be formed
 - 7 that includes the first and second digital circuits;
 - 8 operating the first, second, and test clock signals to cause the scan chain to
 - 9 receive test data such that the test clock assumes one state to hold the latch element while
 - 10 the edge-triggered devices are caused to change state by the first and second clock signals
 - 11 and the test clock then assumes a second state to allow data to pass along the test path
 - 12 from the one digital circuit to the other.

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